

Phase I Pixel Failure Scenarios

Tamás Álmos VÁMI¹, János KARANCSI²

¹ Wigner RCP, Budapest

² ATOMKI, Debrecen

PPD meeting



Intro

Presentation from me at the Pixel Offline meeting:

<https://indico.cern.ch/event/607513/#29-pixel-failure-scenarios>

Method:

- MC Simulation with 80.000 events (MinBias)
- SiPixelQuality object is used to „kill” the dead parts of the detector
- Occupancy is plotted

<https://twiki.cern.ch/twiki/bin/view/CMS/SiPixelPhase1FailureScenarios>

<https://tvami.web.cern.ch/tvami/projects/Phase1FailureScenarios/>

Scenarios

Scenario 0: Perfect Detector (New cabling map validation)

Scenario 1: Random 5%

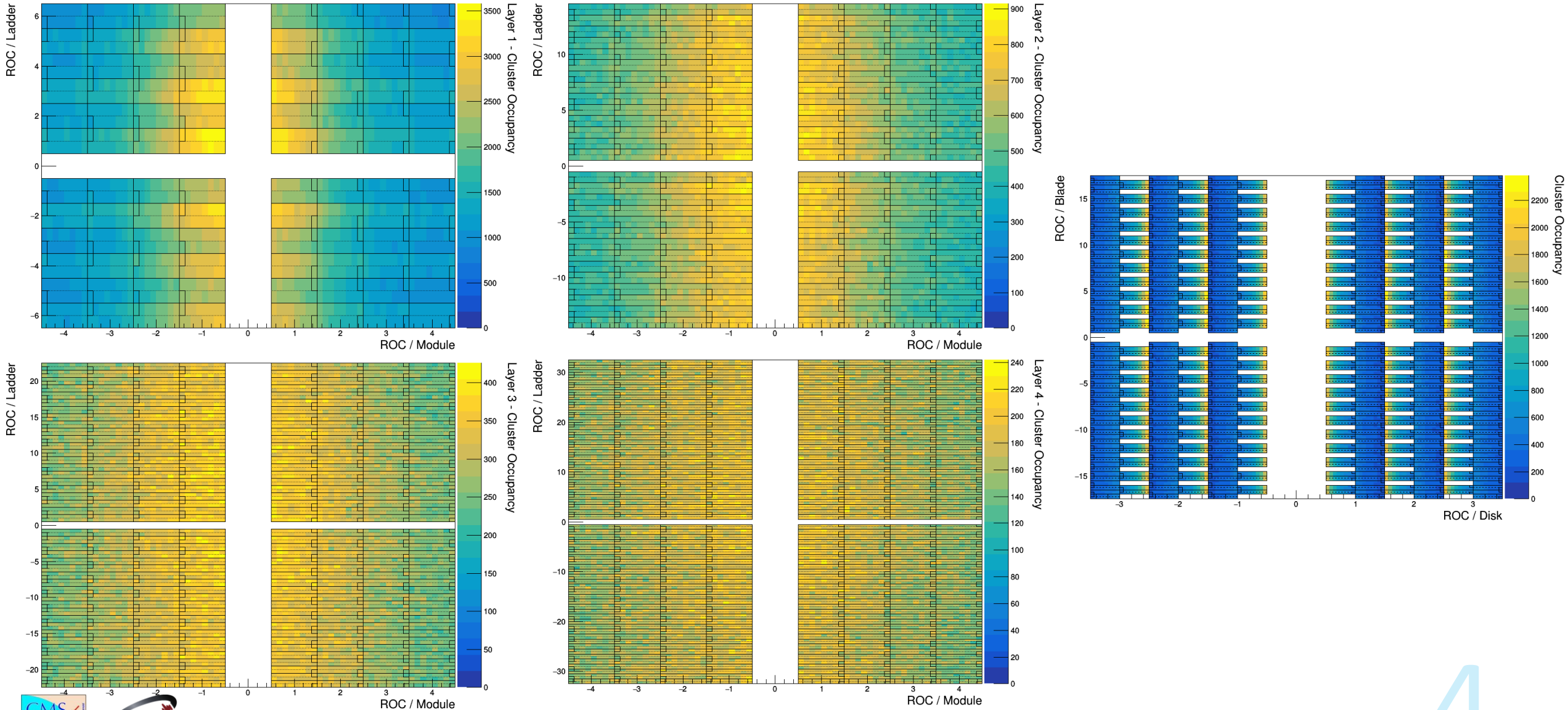
Scenario 2: 1 BPix + 1 FPix cooling loop out

Scenario 3: BmO SEC4 L1+L4 out,
BpI SEC6 L2+L3 out,
BmI Disk1 ROG3 HV2 out
BpO Disk2 ROG1 HV1 out

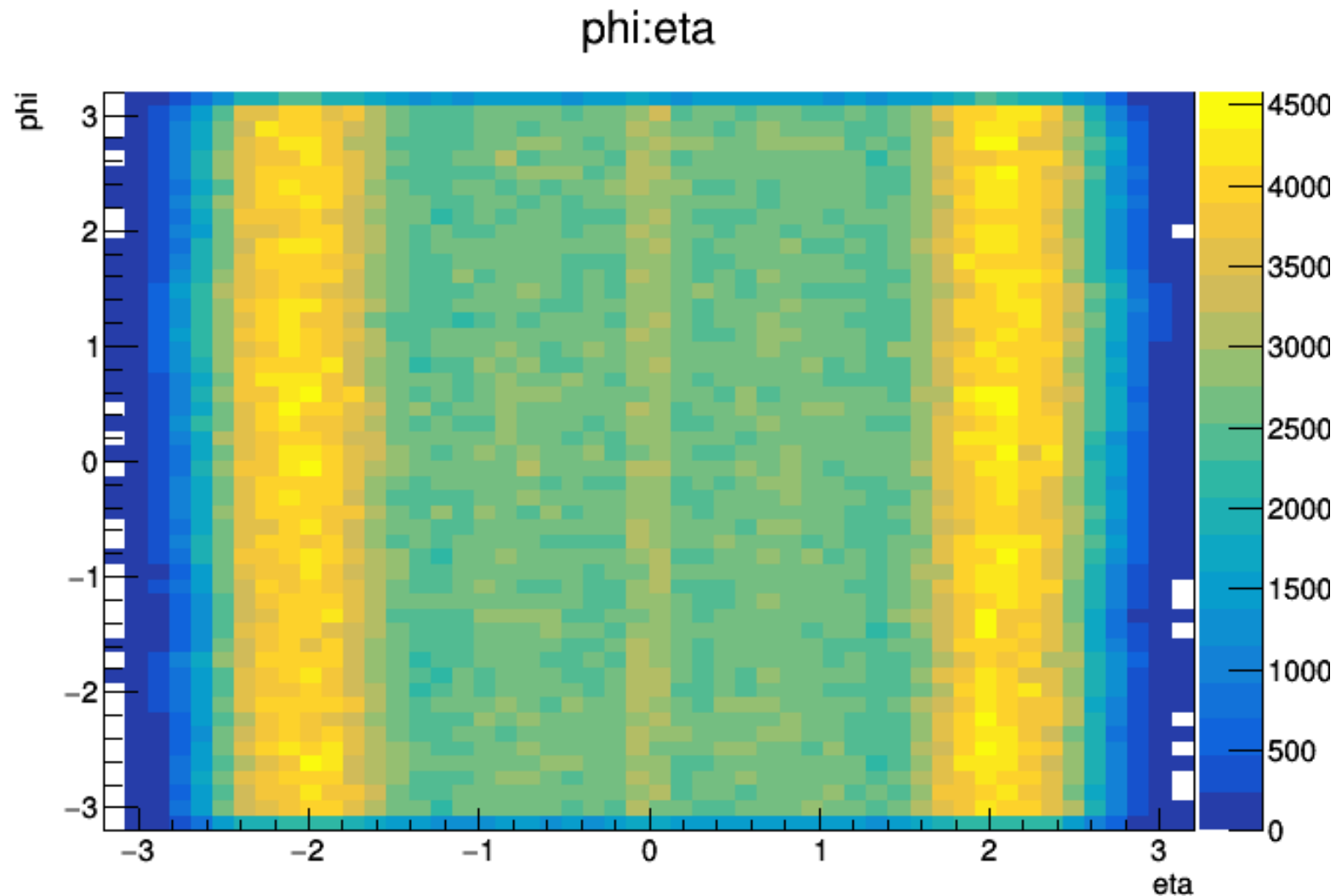
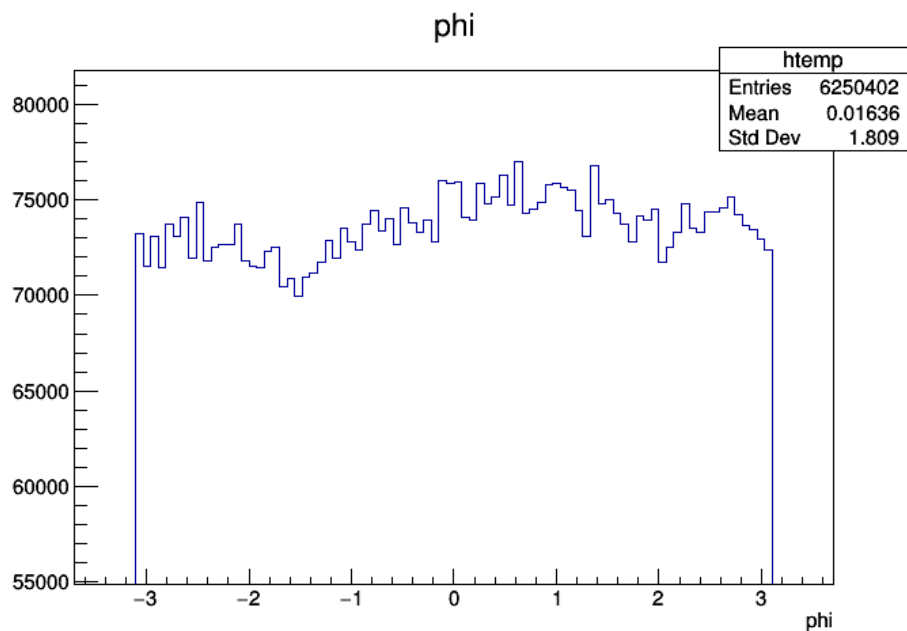
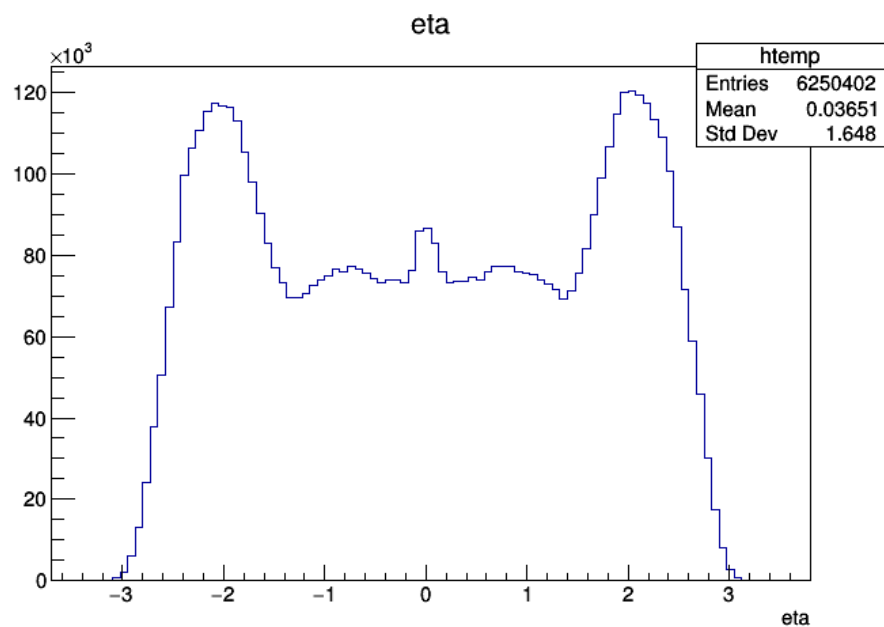
Scenario 4: 1 BPix + 1 FPix FED out

Scenario 5: 1 BPix Read-Out group is out

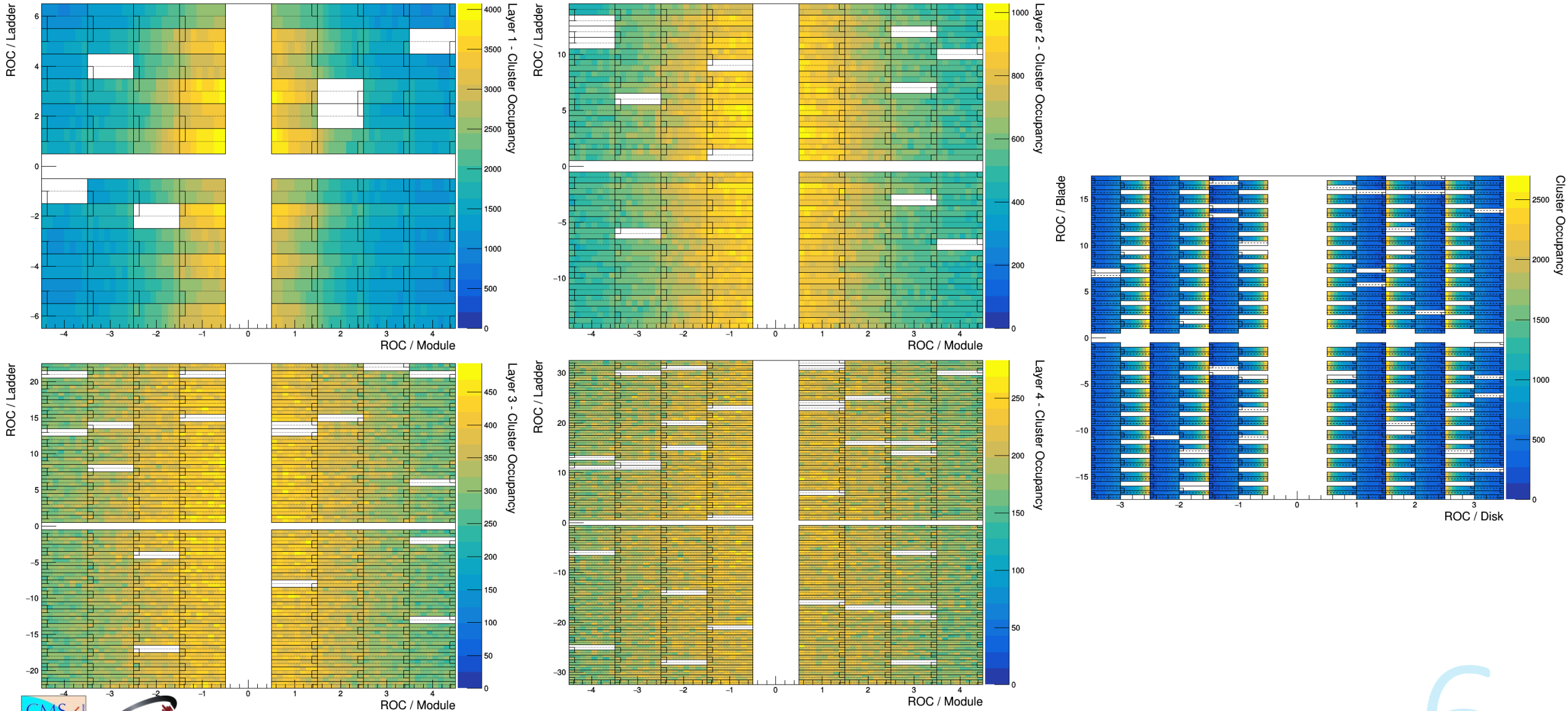
Scenario 0: Perfect detector



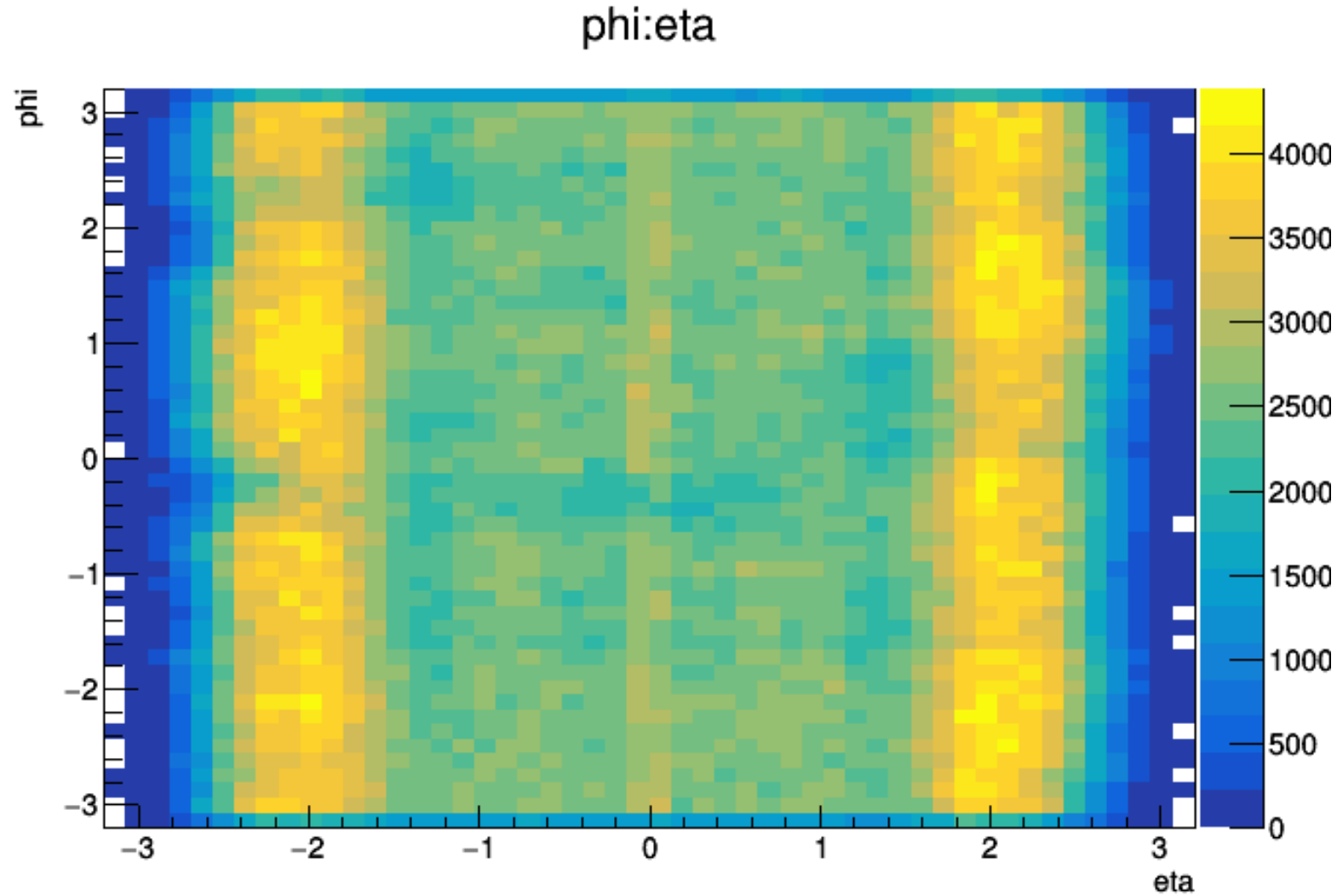
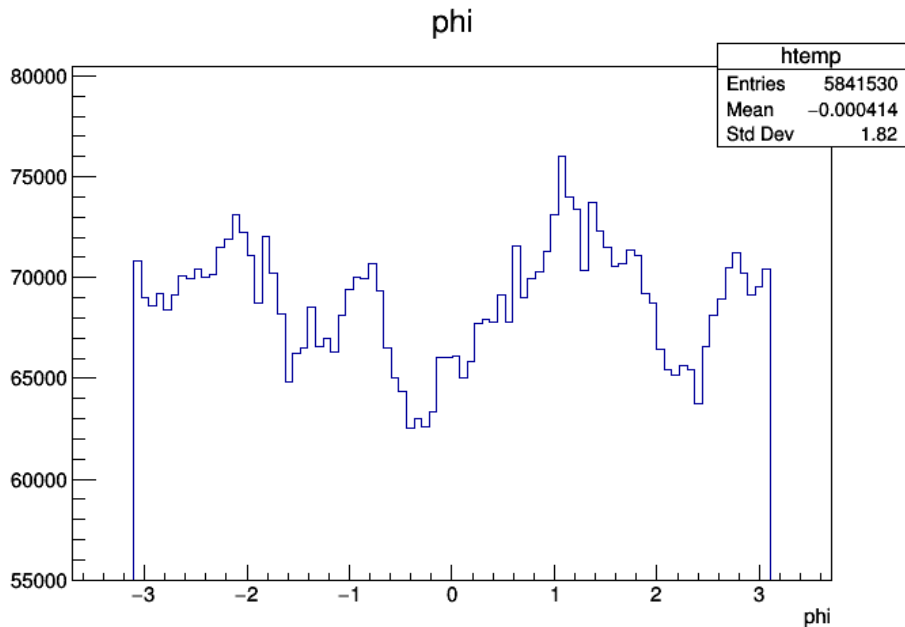
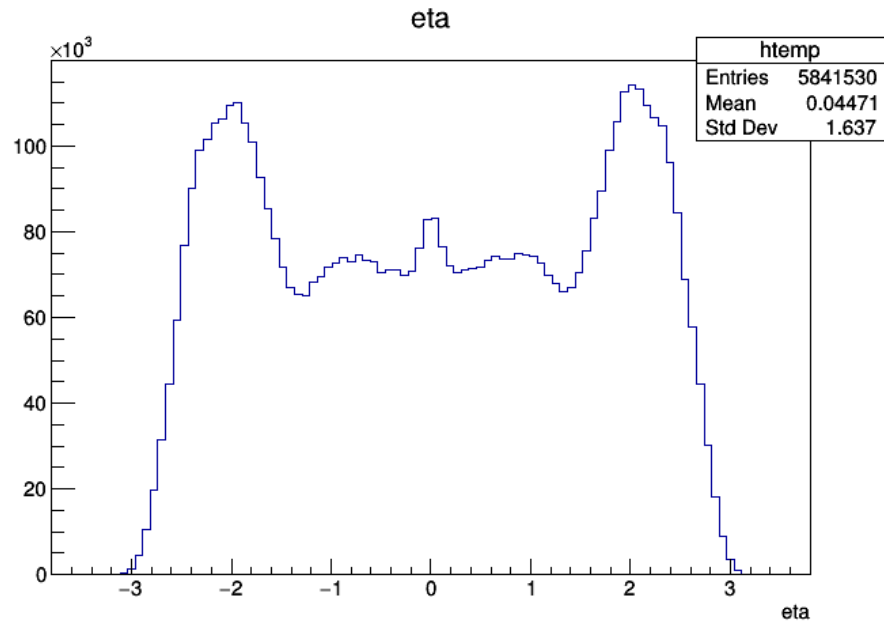
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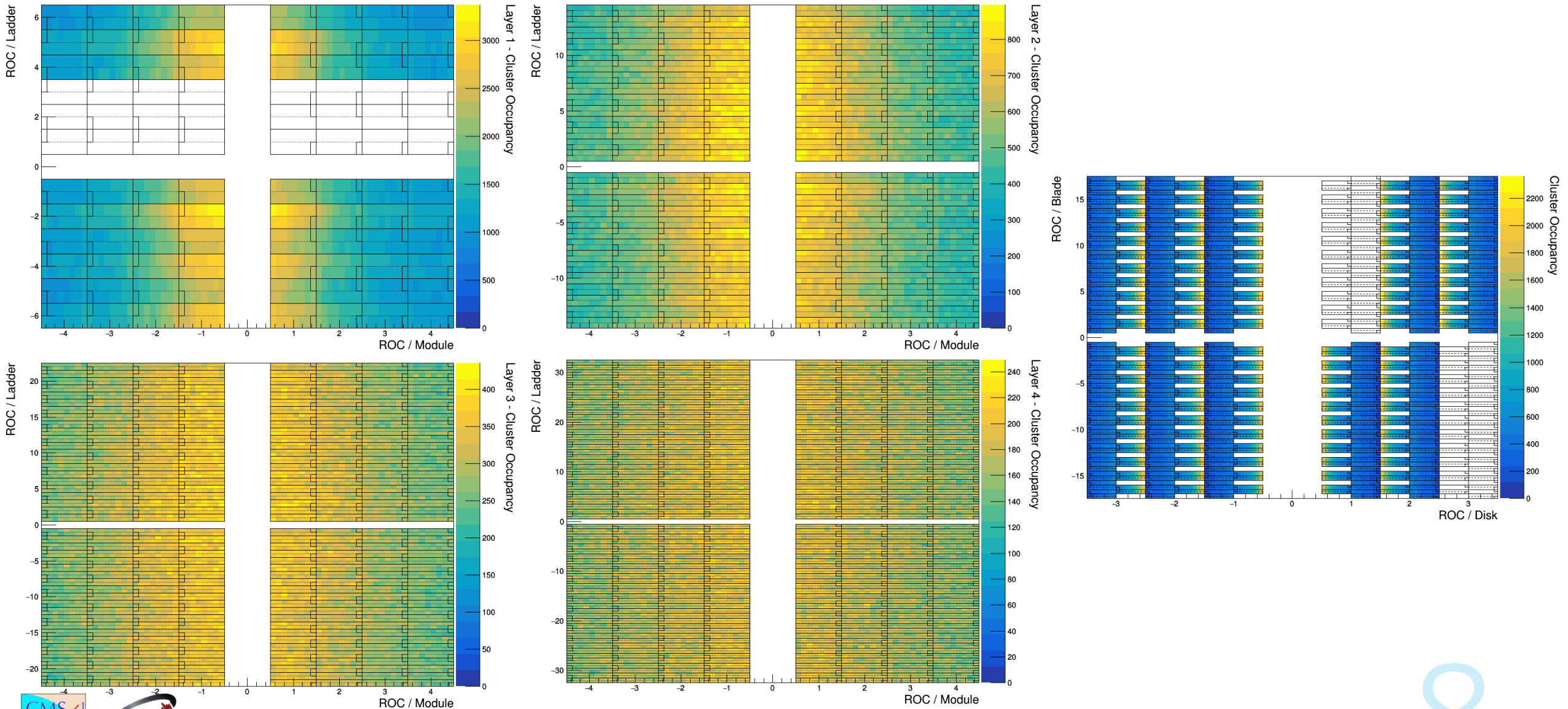
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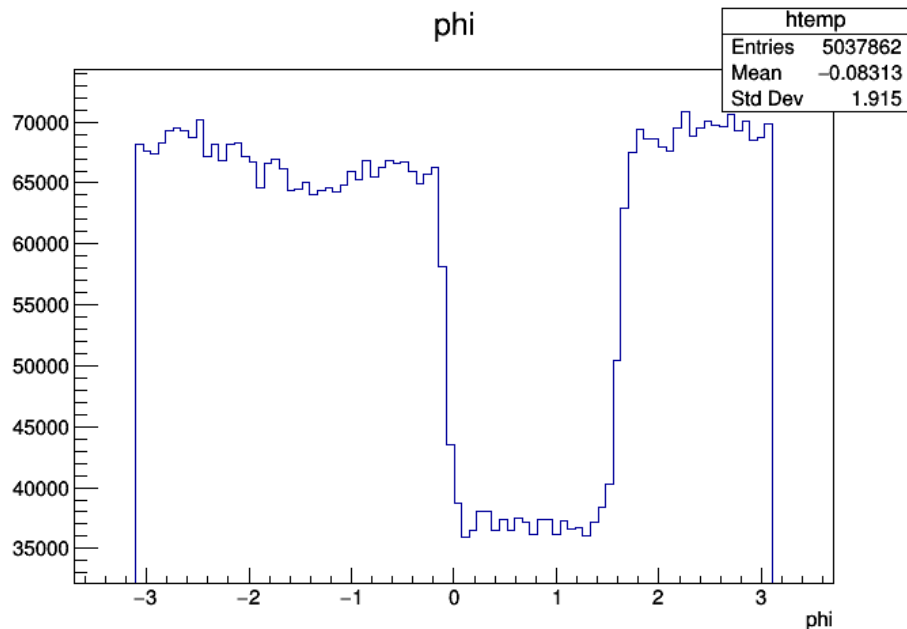
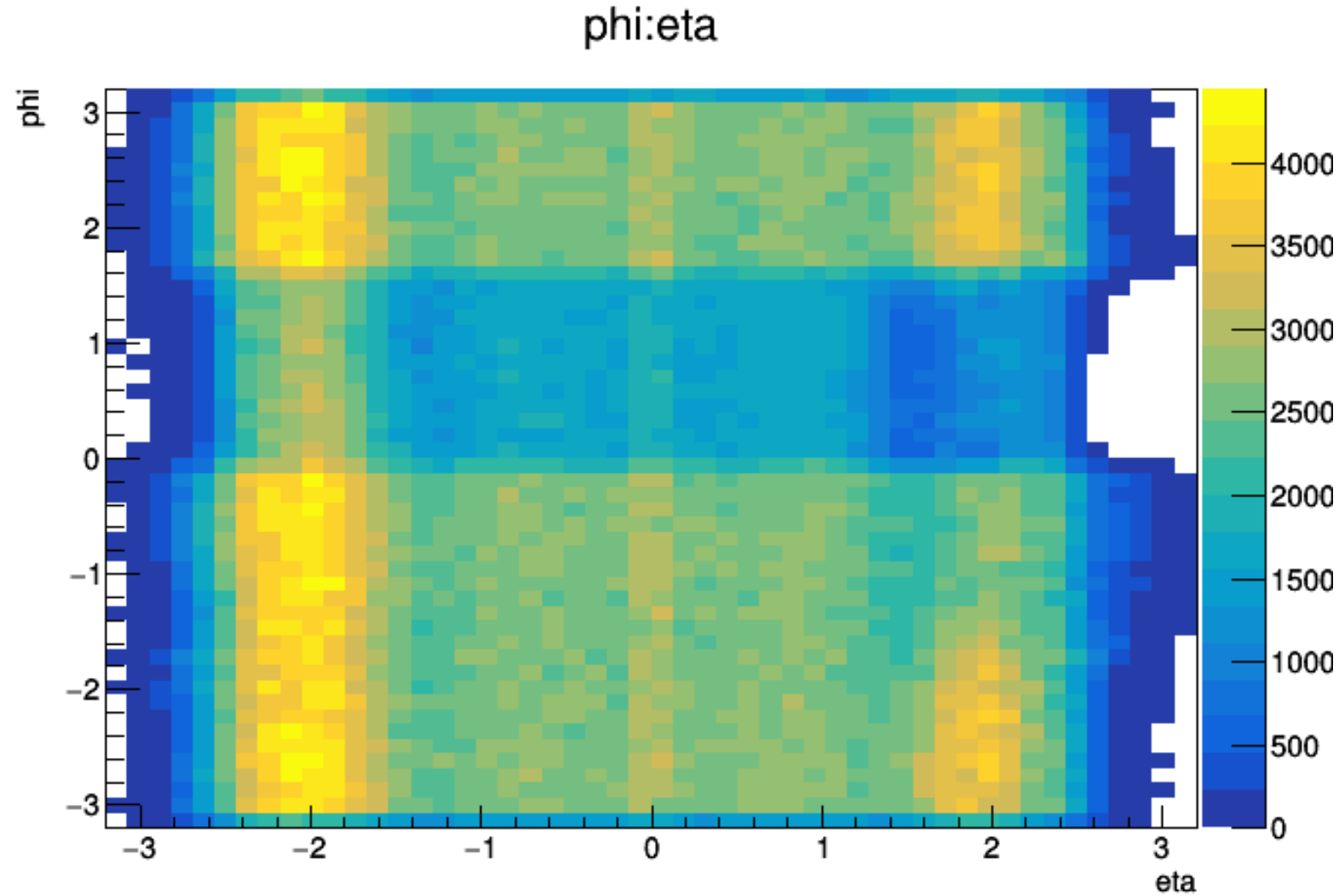
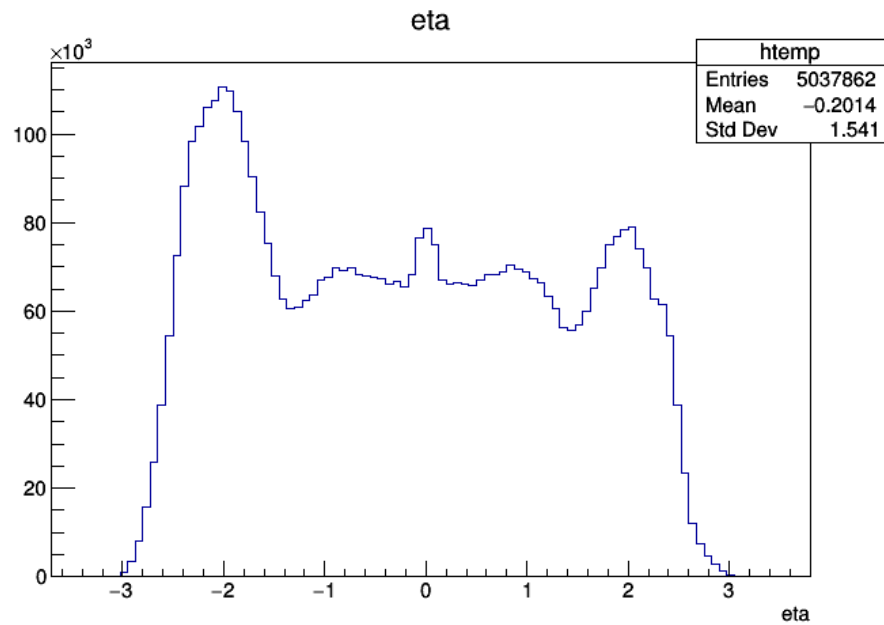
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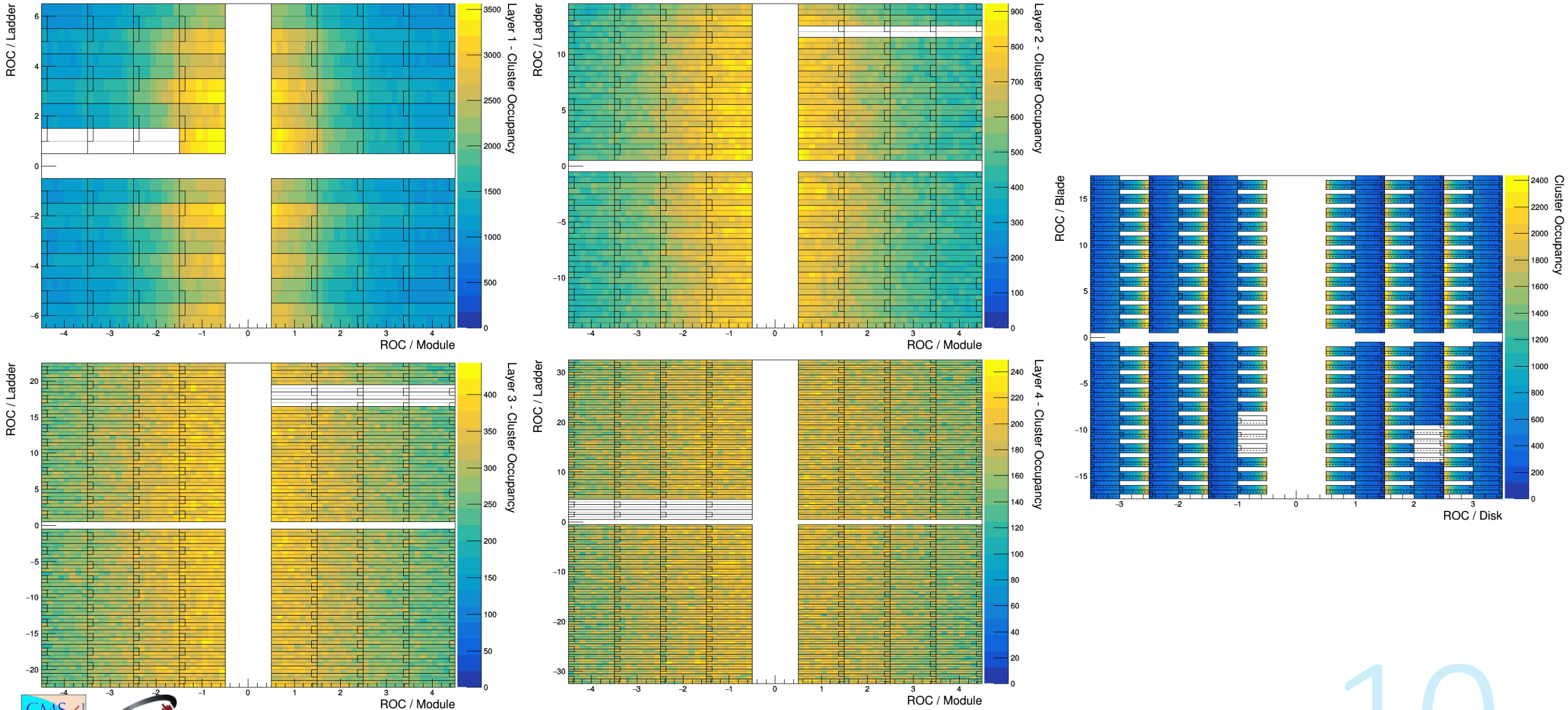
Scenario 2: 1 BPix + 1 FPix cooling loop



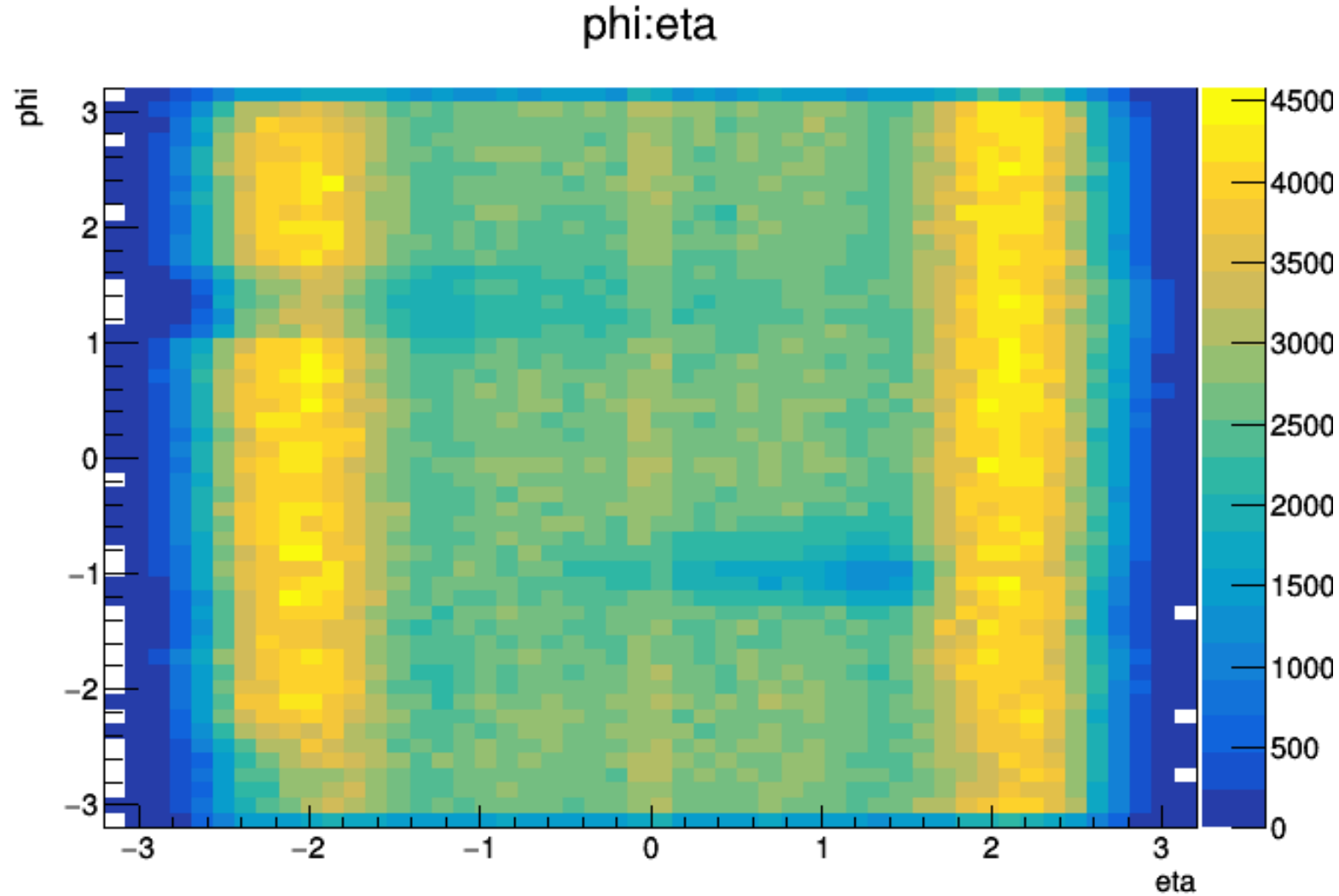
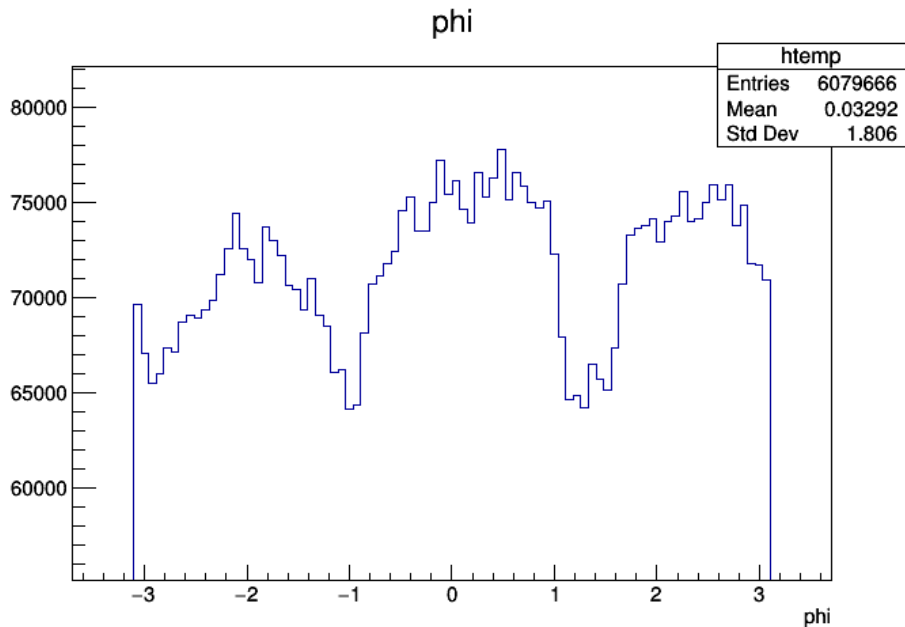
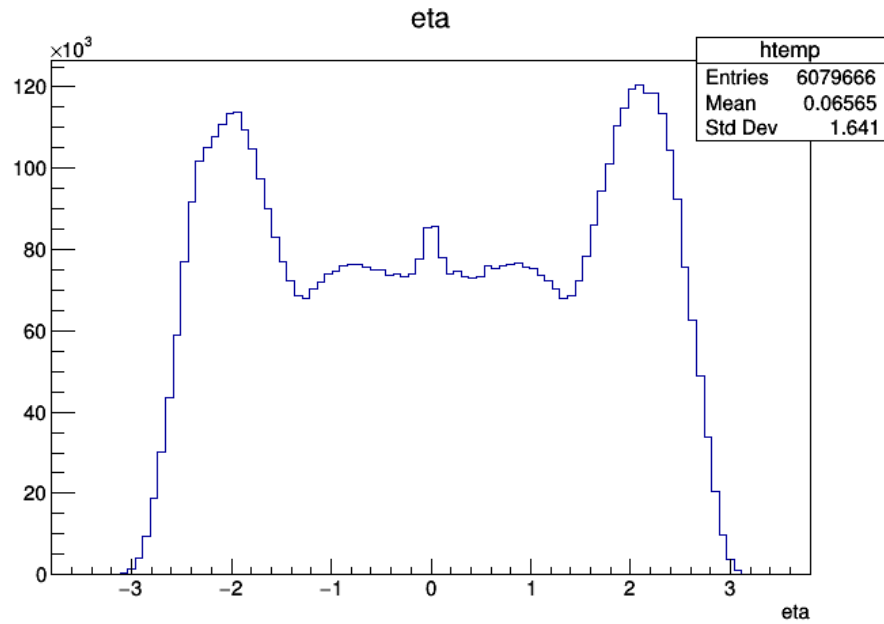
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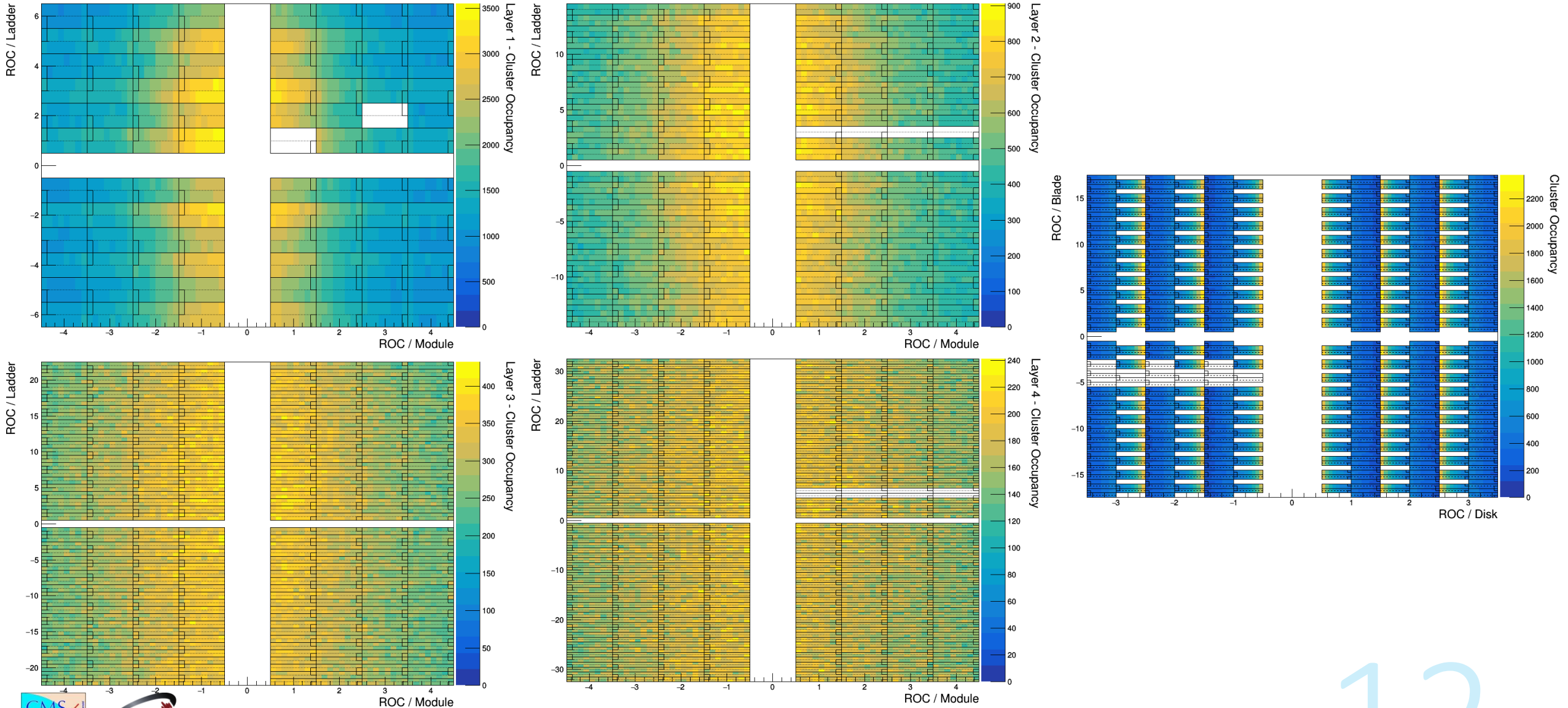
Scenario 3: HV group out



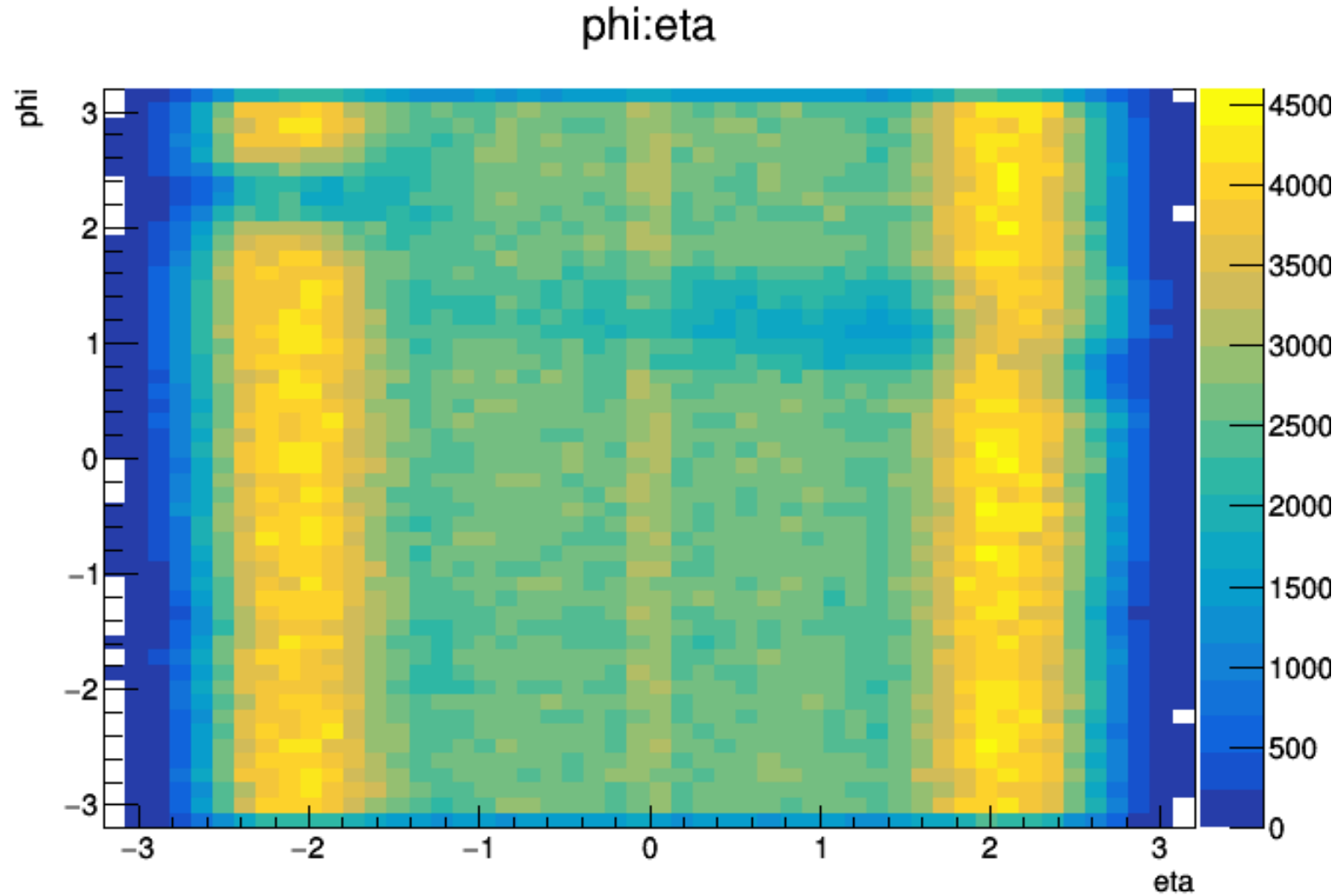
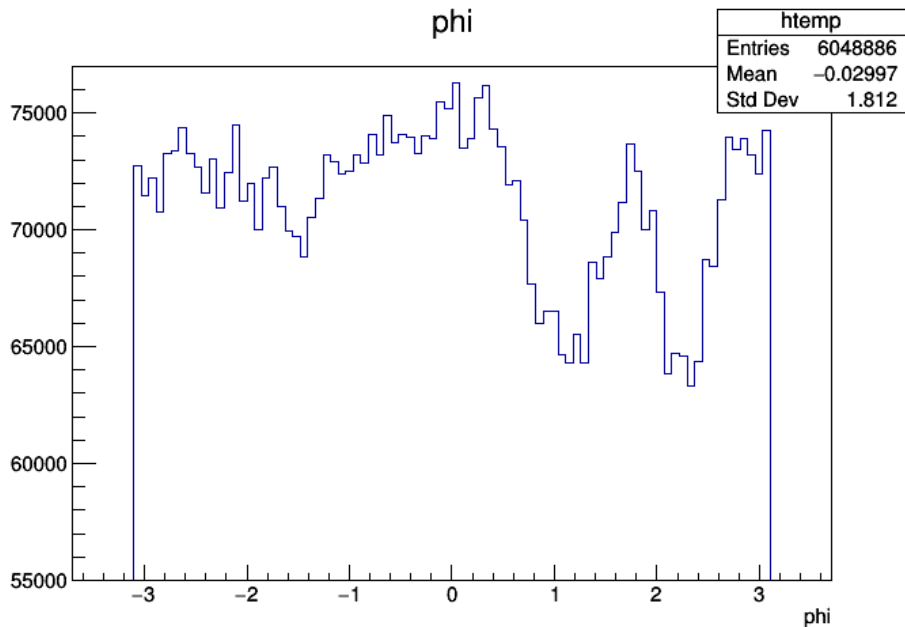
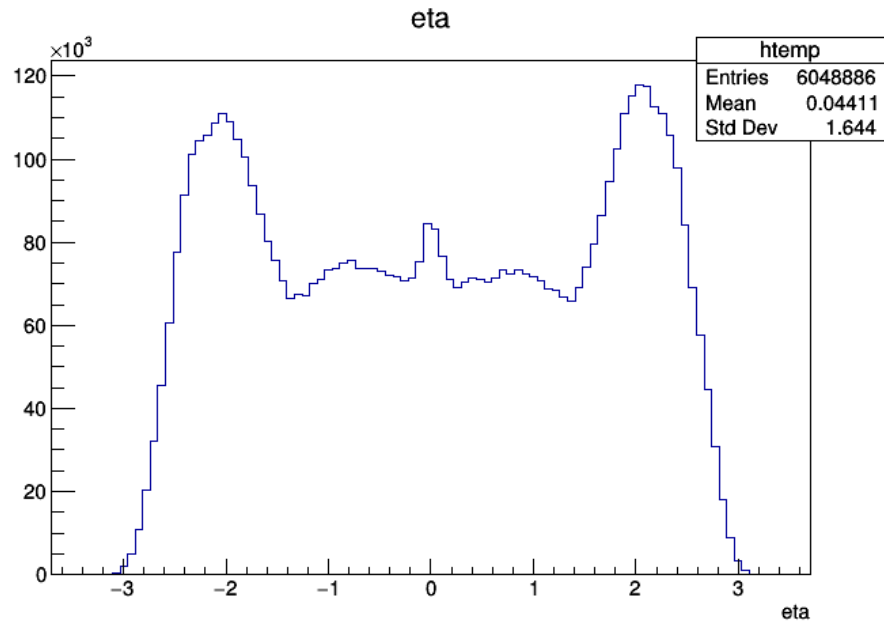
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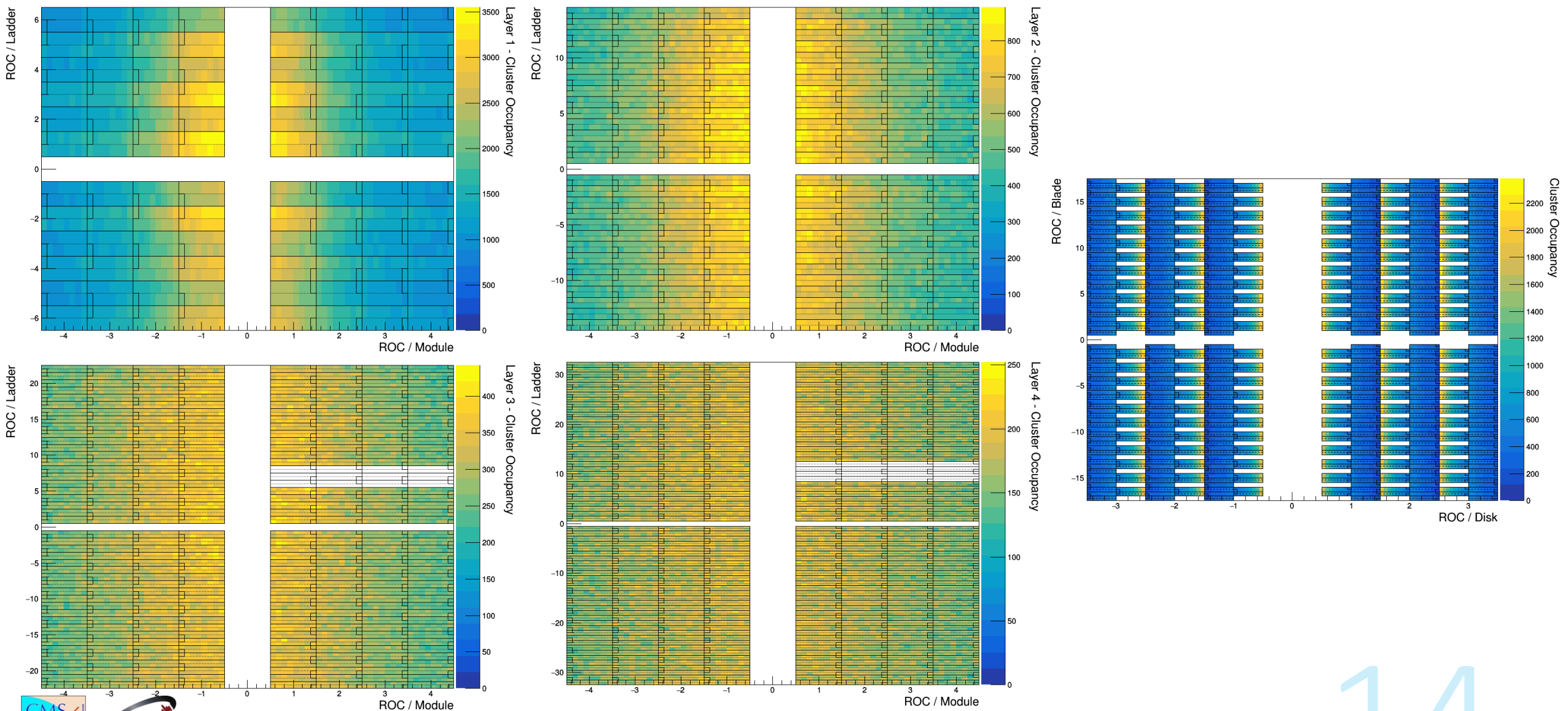
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Scenario 5: Read-Out group out



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