Phase I Failure Scenarios

Tamás Álmos VÁMI[1], János KARANCSI[2]

[1] Wigner RCP, Budapest
[2] ATOMKI, Debrecen

Pixel Online meeting

Intro

Presentation from Janos:
https://indico.cern.ch/event/602634/contributions/2431075/attachments/1393899/2124262/2017_01_11_PixelOfflineMeeting_PixelFailureScenarios.pdf

Validation plots presentation:
https://indico.cern.ch/event/607513/#29-pixel-failure-scenarios

https://twiki.cern.ch/twiki/bin/view/CMS/SiPixelPhase1FailureScenarios

https://tvami.web.cern.ch/tvami/projects/Phase1FailureScenarios/

Scenarios

Scenario 1: Random 5%
Scenario 2: 1 BPix + 1 FPix cooling loop out (FPix validation in progress)
Scenario 3: BmO SEC4 L1+L4 out,
BpI SEC6 L2+L3 out,
BmI Disk1 ROG3 HV2 out
BpO Disk2 ROG1 HV1 out
Scenario 4: 1 BPix + 1 FPix FED out